SEMICONDUCTOR DEVICE

CROSS-REFERENCE TO RELATED APPLICATION

This application is based upon and claims the benefit of priority from Japanese Patent Application No. 2015-179161; filed on September 11, 2015; the entire contents of which are incorporated herein by reference.

FIELD

Embodiments described herein relate generally to a semiconductor device.

BACKGROUND

For miniaturization or high performance of a transistor, a vertical transistor having a gate electrode buried in a trench is used. In the vertical transistor, drain-source breakdown voltage (hereinafter, also referred to as “breakdown voltage”) and ON resistance are in a trade-off relationship. That is, if impurity concentration of a drift layer increases to decrease the ON resistance, the breakdown voltage decreases. In contrary to this, if the impurity concentration of the drift layer decreases to increase the breakdown voltage, the ON resistance increases.

There is a structure in which a field plate electrode is provided on a lower side of a gate electrode in a trench, as a method of improving the trade-off between breakdown voltage and ON resistance. An electric field distribution of a drift layer is changed by a field plate electrode, and thereby breakdown voltage of a vertical transistor increases, while impurity concentration of a drift layer is maintained as it is. Further improvement of the trade-off between the breakdown voltage and the ON resistance of the vertical transistor is required.

An example of the related art includes JP-A-2014-225693.

DESCRIPTION OF THE DRAWINGS

FIG. 1 is a schematic sectional view of a semiconductor device according to a first embodiment.

FIGS. 2A and 2B are explanatory diagrams illustrating action and effect of the semiconductor device according to the first embodiment.

FIG. 3 is another explanatory diagram illustrating action and effect of the semiconductor device according to the first embodiment.

FIGS. 4A and 4B are yet another explanatory diagrams illustrating action and effect of the semiconductor device according to the first embodiment.

FIGS. 5A and 5B are yet another explanatory diagrams illustrating action and effect of the semiconductor device according to the first embodiment.

FIG. 6 is a schematic sectional view of a semiconductor device according to a second embodiment.

DETAILED DESCRIPTION

[0005]Exemplary embodiments provide a semiconductor device which can improve trade-off between breakdown voltage and ON resistance of a vertical transistor.

[0006]In generatl, according to one embodiment, a semiconductor device includes a semiconductor layer having a first surface and a second surface, a drift region of a first conductivity type which is provided in the semiconductor layer, a body region of a second conductivity type which is provided in the semiconductor layer between the drift region and the first surface, a source region of first conductivity type which is provided in the semiconductor layer between the body region and the first surface, a first gate electrode, a second gate electrode which is provided interposed with the body region between the first gate electrode and the second gate electrode, a first gate insulating film which is provided between the first gate electrode and the body region, a second gate insulating film which is provided between the second gate electrode and the body region, a first field plate electrode which is provided between the second surface and the first gate electrode, a second field plate electrode which is provided between the second surface and the second gate electrode, a first field plate insulating film which is provided between the first field plate electrode and the drift region, a second field plate insulating film which is provided between the second field plate electrode and the drift region, a first region of the first conductivity type at least a portion of which is provided in the drift region between the first field plate electrode and the second field plate electrode, a second region which is provided in the drift region between the first region and the body region and has a higher impurity concentration of the first conductivity type than that of the first region, and a third region which is provided in the drift region between the second region and the body region and has a lower impurity concentration of the first conductivity type than that of the second region.

[0008]Hereinafter, embodiments of the invention will be described with reference to the accompanying drawings. In the following description, the same symbols or reference numerals will be attached to the same or similar members or the like, and description with regard to the members or the like described once will be omitted.

[0009]In addition, in the following description, notation n+, n, n-, p+, and p indicates a relative level of impurity concentration of each conductivity type. That is, n+ indicates that n-type impurity concentration of n+ is relatively higher than that of n, and n- indicates that n-type impurity concentration of n- is relatively lower than that of n. In addition, p+ indicates that p-type impurity concentration of p+ is relatively higher than that of p. There is a case in which an n+-type and an n--type are simply described as an n-type, and a p+-type is simply described as a p-type.

[0010]Impurity concentration can be measured by, for example, secondary ion mass spectrometry (SIMS). In addition, a relative level of impurity concentration can also be determined from a level of carrier concentration which is calculated by, for example, scanning capacitance microscopy (SCM). In addition, a position of a depth direction of an impurity region can be obtained from a combined image of an SCM image and an atomic force microscopy (AFM) image.

First Embodiment

[0011]A semiconductor device according to the present embodiment includes a semiconductor layer having a first surface and a second surface, a drift region of a first conductivity type which is provided in the semiconductor layer, a body region of a second conductivity type which is provided in the semiconductor layer between the drift region and the first surface, a source region of the first conductivity type which is provided in the semiconductor layer between the body region and the first surface, a first gate electrode, a second gate electrode in which the body region is provided between the first gate electrode and the second gate electrode, a first gate insulating film which is provided between the first gate electrode and the body region, a second gate insulating film which is provided between the second gate electrode and the body region, a first field plate electrode which is provided between the second surface and the first gate electrode, a second field plate electrode which is provided between the second surface and the second gate electrode, a first field plate insulating film which is provided between the first field plate electrode and the drift region, a second field plate insulating film which is provided between the second field plate electrode and the drift region, a first region of the first conductivity type which is provided inside the drift region between the first field plate electrode and the second field plate electrode, a second region which is provided in the drift region between the first region and the body region and has a higher impurity concentration of the first conductivity type than that of the first region, and a third region a second region which is provided in the drift region between the second region and the body region and has a lower impurity concentration of the first conductivity type than that of the second region.

[0012]FIG. 1 is a schematic sectional view of a semiconductor device according to a first embodiment. The semiconductor device 100 according to the present embodiment is a vertical metal oxide semiconductor field effect transistor (MOSFET) which has a gate electrode inside a trench. Hereinafter, a case in which a first conductivity type is an n-type and a second conductivity type is a p-type, that is, a case of an n channel type MOSFET will be described as an example.

[0013]The MOSFET 100 according to the present embodiment includes a silicon layer (semiconductor layer) 10. The silicon layer 10 includes an n+-type drain region 12, an n--type or an n-type drift region 14, a p-type body region 16, an n+-type source region 18, and a p+-type body contact region 20. The n--type or an n-type drift region 14 includes an n--type lower portion region (first region) 14a, an n-type intermediate region (second region) 14b, and an n--type upper portion region (third region) 14c.

[0014]In addition, the MOSFET 100 includes a first gate electrode 22, a second gate electrode 23, a first gate insulating film 24, a second gate insulating film 25, a first field plate electrode 26, a second field plate electrode 27, a first field plate insulating film 28, a second field plate insulating film 29, a first insulating film 30, a second insulating film 31, an interlayer insulating film 32, a source electrode 34, and a drain electrode 36. In addition, the MOSFET 100 includes a first trench 40 and a second trench 41.

[0015]The silicon layer 10 includes a first surface and a second surface. Hereinafter, the first surface is referred to as a front surface, and the second surface is referred to as a rear surface.

[0016]The silicon layer 10 is silicon (Si) of a single crystal. A surface of the silicon layer 10 is tilted by degrees greater than or equal to zero degree and less than or equal to eight degrees, with respect to (100) plane.

[0017]The n+-type drain region 12 is provided inside the silicon layer 10. The n+-type drain region 12 contains n-type impurity. The n-type impurity is, for example, phosphorus (P) or arsenic (As). For example, impurity concentration of an n-type is greater than or equal to 1´1018 cm-3 and less than or equal to 1´1021 cm-3.

[0018]The the drift region 14 of an n--type or an n-type is provided inside the silicon layer 10. The drift region 14 is provided on the n+-type drain region 12. The drift region 14 contains n-type impurity. The n-type impurity is, for example, phosphorus (P) or Arsenic (As). For example, impurity concentration of an n-type is greater than or equal to 1´1014 cm-3 and less than or equal to 1´1017 cm-3. The drift region 14 is, for example, an epitaxial growth layer which is formed on the n+-type drain region 12 by epitaxial growth.

[0019]The drift region 14 includes the n--type lower portion region 14a, the n-type intermediate region 14b, and the n--type upper portion region 14c. At least a portion of the n--type lower portion region 14a is provided between the first field plate electrode 26 and the second field plate electrode 27.

[0020]The intermediate region 14b is provided between the lower portion region 14a and the p-type body region 16. The n-type impurity concentration of the intermediate region 14b is greater than n-type impurity concentration of the lower portion region 14a. The intermediate region 14b has the peak of impurity distribution of n-type impurity.

[0021]The intermediate region 14b is formed by performing, for example, ion injection of n-type impurity onto the drift region 14. For example, the intermediate region 14b can also be formed at the same time when the drift region 14 is formed by epitaxial growth.

[0022]The upper portion region 14c is provided between the intermediate region 14b and the body region 16. The intermediate region 14b is interposed between the lower portion region 14a and the upper portion region 14c. The n-type impurity concentration of the upper portion region 14c is lower than that of the intermediate region 14b.

[0023]The n-type impurity concentration of the intermediate region 14b is, for example, higher than or equal to 1.5 times and lower than or equal to 10 times the n-type impurity concentration of the lower portion region 14a. The n-type impurity concentration of the intermediate region 14b is, for example, higher than or equal to 1.5 times and lower than or equal to 10 times the n-type impurity concentration of the upper portion region 14c.

[0024]The n-type impurity concentration of the intermediate region 14b which becomes a comparative target is a maximum of n-type impurity concentration, that is, the peak value of the concentration distribution of the n-type impurity. In addition, the n-type impurity concentrations of the lower portion region 14a and the upper portion region 14c is set to n-type impurity concentration of an end portion of hem of concentration distribution leading from the peak of the n-type impurity concentration of the intermediate region 14b.

[0025]For example, n-type impurity concentration of the lower portion region 14a is the same as that of the upper portion region 14c.

[0026]The intermediate region 14b is provided between the first field plate electrode 26 and the second field plate electrode 27.

[0027]In addition, for example, a position in which n-type impurity concentration of the intermediate region 14b is the maximum is placed between two surfaces which are obtained by equally dividing the drift region 14 between a surface parallel with a rear surface of the silicon layer 10 including an end portion on a rear surface side of the first field plate electrode 26, and a surface parallel with a rear surface of the silicon layer 10 including a boundary between the drift region 14 and the p type body region 16, into three regions.

[0028]The p type body region 16 is provided inside the silicon layer 10 between the drift region 14 and a front surface of the silicon layer 10. When the MOSFET 100 is turned on, a channel is formed in a region which comes into contact with the first gate insulating film 24 and the second gate insulating film 25.

[0029]The body region 16 contains p type impurity. The p type impurity is, for example, boron (B). For example, the p type impurity concentration is greater than or equal to 1´1016 cm-3 and less than or equal to 1´1018 cm-3.

[0030]The n+-type source region 18 is provided inside the silicon layer 10 between the body region 16 and a front surface (first surface) of the silicon layer 10. The source region 18 contains n-type impurity. The n-type impurity is, for example, phosphorus (P) or arsenic (As). For example, the n-type impurity concentration is greater than or equal to 1´1019 cm-3 and less than or equal to 1´1021 cm-3.

[0031]The p+-type body contact region 20 is provided inside the silicon layer 10 between the body region 16 and the first surface. The body contact region 20 is interposed between two source regions 18.

[0032]The body contact region 20 contains p type impurity. For example, the p type impurity is boron (B). For example, the p type impurity concentration is greater than or equal to 1´1019 cm-3 and less than or equal to 1´1021 cm-3.

[0033]The first gate electrode 22 is provided inside the first trench 40. For example, the first gate electrode 22 is formed of polycrystalline silicon containing n-type impurity or p type impurity.

[0034]The second gate electrode 23 is provided inside the second trench 41. The body region 16 is interposed between the second gate electrode 23 and the first gate electrode 22.

[0035]The first gate insulating film 24 is provided between the first gate electrode 22 and the body region 16. The first gate insulating film 24 is, for example, a silicon oxide film.

[0036]The second gate insulating film 25 is provided between the second gate electrode 23 and the body region 16. The second gate insulating film 25 is, for example, a silicon oxide film.

[0037]The first field plate electrode 26 is provided inside the first trench 40. The first field plate electrode 26 is provided between the first gate electrode 22 and a rear surface (second surface) of the silicon layer 10.

[0038]The first field plate electrode 26 has a function of changing electric field distribution of the drift region 14 and increasing breakdown voltage of the MOSFET 100, when the MOSFET 100 is turned on. For example, the first field plate electrode 26 is formed of polycrystalline silicon containing n-type impurity or p type impurity.

[0039]The second field plate electrode 27 is provided inside the second trench 41. The second field plate electrode 27 is provided between the second gate electrode 23 and the second surface.

[0040]The second field plate electrode 27 has a function of changing electric field distribution of the drift region 14 and increasing breakdown voltage of the MOSFET 100, when the MOSFET 100 is turned off. For example, the second field plate electrode 27 is formed of polycrystalline silicon containing n-type impurity or p type impurity.

[0041]The first field plate insulating film 28 is provided between the first field plate electrode 26 and the drift region 14. The first field plate insulating film 28 is, for example, a silicon oxide film.

[0042]The second field plate insulating film 29 is provided between the second field plate electrode 27 and the drift region 14. The second field plate insulating film 29 is, for example, a silicon oxide film.

[0043]The first insulating film 30 is provided between the first gate electrode 22 and the first field plate electrode 26. The first insulating film 30 has a function of electrically decoupling the first gate electrode 22 from the first field plate electrode 26. The first field plate electrode 26 is fixed to, for example, a ground potential. The first insulating film 30 is, for example, a silicon oxide film.

[0044]The second insulating film 31 is provided between the second gate electrode 23 and the second field plate electrode 27. The second insulating film 31 has a function of electrically decoupling the second gate electrode 23 from the second field plate electrode 27. The second field plate electrode 27 is fixed to, for example, a ground potential. The second insulating film 31 is, for example, a silicon oxide film.

[0045]The interlayer insulating film 32 is provided between the first gate electrode 22 and the source electrode 34. In addition, the interlayer insulating film 32 is provided between the second gate electrode 23 and the source electrode 34. The interlayer insulating film 32 has a function of electrically decoupling the first gate electrode 22 and the source electrode 34 from the second gate electrode 23 and the source electrode 34. The interlayer insulating film 32 is, for example, a silicon oxide film.

[0046]The source electrode 34 is provided on the first surface. The source electrode 34 is electrically coupled to the source region 18 and the body contact region 20. The source electrode 34 comes into contact with the source region 18 and the body contact region 20. The source electrode 34 is a metal electrode. The source electrode 34 is, for example, a laminated film of titanium (Ti) and aluminum (Al).

[0047]The drain electrode 36 is provided on the second surface. The drain electrode 36 is electrically coupled to the drift region 14 and the n+-type drain region 12. The drain electrode 36 comes into contact with the n+-type drain region 12. The drain electrode 36 is a metal electrode. The drain electrode 36 is a laminated film of titanium (Ti), aluminum (Al), nickel (Ni), copper (Cu), silver (Ag), gold (Au) or the like.

[0048]Hereinafter, actions and effects of the semiconductor device according to the present embodiment will be described. FIGS. 2A and 2B, FIG. 3, FIGS. 4A and 4B, and FIGS. 5A and 5B are explanatory diagrams illustrating actions and effects of the semiconductor device according to the present embodiment.

[0049]FIGS. 2A and 2B illustrate simulation results of current-voltage characteristics of the MOSFET. FIGS. 2A and2B illustrate the current-voltage characteristics of the MOSFET of a case in which ion injection of phosphorus (P) is performed onto the n--type drift region 14 by using acceleration energy of 4.0 MeV, and thereby the intermediate region 14b is formed. FIG. 2A illustrates a case in which n-type impurity concentration of the n--type drift region 14 is 1.5´1016 cm-3 before ion injection is performed, and FIG. 2B illustrates a case in which n-type impurity concentration of the n--type drift region 14 is 2.0´1016 cm-3.

[0050]By providing the intermediate region 14b, it is clear that breakdown voltage between a drain and a source increases approximately 5 V as illustrated in FIG. 2, and the drain-source breakdown voltage increases approximately 4 V as illustrated in FIG. 2, compared to a case in which the intermediate region 14b is not provided.

[0051]FIG. 3 illustrates a simulation result of acceleration energy dependence on drain-source breakdown voltage. FIG. 3 illustrates results of a case in which n-type impurity concentration of the n--type drift region 14 is 1.5´1016 cm-3 before ion injection is performed and a case in which n-type impurity concentration of the n--type drift region 14 is 2.0´1016 cm-3. Acceleration energy is changed in a range of 0.8 MeV to 4.0 MeV.

[0052]Regardless of the concentration of the drift region 14, drain-source pressure resistance increase in accordance with an increase of the acceleration energy. That is, as the depth from a front surface of the silicon layer 10 of the intermediate region 14b increases, drain-source breakdown voltage is increased. Particularly, if the acceleration energy is 3.2 MeV or more, the drain-source breakdown voltage is remarkably increased, compared o a case in which the intermediate region 14b is not provided.

[0053]FIGS. 4A and 4B illustrate simulation results of acceleration energy dependence of distribution of n-type impurity concentration in a depth direction and electric field distribution in a depth direction. FIG. 4A illustrates distribution of n-type impurity concentration, and FIG. 4B illustrates electric field distribution. FIGS. 4A and 4B illustrate a case in which n-type impurity concentration of the drift region 14 of an n--type is 1.5´1016 cm-3, before ion injection is performed.

[0054]As illustrated in FIG. 4A, as acceleration energy increases, a position in which n-type impurity concentration of the intermediate region 14b is the maximum becomes deeper. A maximum value of n-type impurity concentration of the intermediate region 14b is in a range from concentration higher than or equal to 3´1016 cm-3 to concentration lower than or equal to 5´1016 cm-3. The maximum value is in a range from two times to four times the n-type impurity concentrations of the lower portion region 14a and the upper portion region 14c.

[0055]It is preferable that a position in which n-type impurity concentration of the intermediate region 14b is the maximum is a position between two surfaces which are obtained by equally dividing the drift region 14 between a surface parallel with a rear surface of the silicon layer 10 including an end portion on a rear surface side of the first field plate electrode 26, and a surface parallel with a rear surface of the silicon layer 10 including a boundary between the drift region 14 and the p type body region 16, into three regions. That is, it is preferable that the position in which n-type impurity concentration of the intermediate region 14b is the maximum is placed in a range denoted by a double-headed arrow in FIG. 4A.

[0056]The position in which n-type impurity concentration of the intermediate region 14b is the maximum is included in the above-described range, and thus drain-source breakdown voltage is remarkably increased, compared to a case in which the intermediate region 14b is not provided.

[0057]As illustrated in FIG. 4B, if ion injection is not performed, that is, if the intermediate region 14b is not provided, the electric field distribution has the peak at a boundary between the drift region 14 and the p type body region 16, and both end portions on the bottom side of the trench of the first field plate electrode 26, and an intermediate portion between two peaks exhibits a concave shape.

[0058]By performing ion injection and providing the intermediate region 14b, electric field strength of the intermediate portion exhibiting the concave shape is raised. Thus, acceleration energy of ion injection increases, and raising degrees of the electric field strength of the intermediate portion increases. The drain-source breakdown voltage is an integral value of the electric field strength in a depth direction. In the present embodiment, by providing the intermediate region 14b, the electric field strength is raised, an integral value of the electric field strength in a depth direction is increased, and the drain-source breakdown voltage is increased.

[0059]FIGS. 5A and 5B illustrate simulation results of distribution of n-type impurity concentration and electric field distribution in a depth direction. FIGS. 5A and 5B illustrate only a case in which the acceleration energy is 4.0 MeV. FIG. 5A illustrates the distribution of the n-type impurity concentration, and FIG. 5B illustrates the electric field distribution. FIGS. 5A and 5B illustrate a case in which n-type impurity concentration of the drift region 14 of an n--type is 2´1016 cm-3, before ion injection is performed.

[0060]As illustrated in FIG. 5A, a maximum value of the n-type impurity concentration of the intermediate region 14b is in a range from concentration higher than or equal to 3´1016 cm-3 to concentration lower than or equal to 4´1016 cm-3. The maximum value is in a range from 1.5 times to two times the n-type impurity concentrations of the lower portion region 14a and the upper portion region 14c.

[0061]As illustrated in FIG. 5B, in the same manner as in a case of FIG. 4B, by providing the intermediate region 14b, electric field strength is raised in the vicinity of an intermediate portion between a boundary between the drift region 14 and the p type body region 16, and an end portion on a rear surface side of the first field plate electrode 26. For this reason, drain-source breakdown voltage is increased.

[0062]In the MOSFET 100, the intermediate region 14b having higher n-type impurity concentration that those of the lower portion region 14a and the upper portion region 14c are placed between the lower portion region 14a and the upper portion region 14c. For this reason, resistance of the drift region 14, a so-called mesa region, interposed between the first trench 40 and the second trench 41, is decreased, compared to a case in which the intermediate region 14b is not provided. Thus, the drain-source breakdown voltage increases, and ON resistance is reduced.

[0063]It is preferable that n-type impurity concentration of the intermediate region 14b is higher than or equal to 1.5 times and lower than or equal to 10 times the n-type impurity concentration of the n--type lower portion region 14a. In addition, it is preferable that the n-type impurity concentration of the intermediate region 14b is higher than or equal to 1.5 times and lower than or equal to 10 timed the n-type impurity concentration of the upper portion region 14c. If the n-type impurity concentration of the intermediate region 14b is below the range, there is a possibility that a sufficient breakdown voltage increasing effect is not obtained. In addition, if the n-type impurity concentration of the intermediate region 14b is above the range, a slope of electric potential distribution becomes steep, and thus electric field strength becomes too strong, and in contrary to this, there is a possibility that breakdown voltage is degraded.

[0064]As described above, the MOSFET 100 according to the present embodiment can realize an increase of the drain-source breakdown voltage and a decrease of the ON resistance at the same time. Thus, according to the MOSFET 100, it is possible to improve trade-off between breakdown voltage of a vertical transistor and ON resistance.

Second Embodiment

[0065]A semiconductor device according to the present embodiment is the same as the semiconductor device according to the first embodiment except that the semiconductor device according to the present embodiment does not include the first insulating film and the second insulating film. Thus, description with regard to content which overlaps that of the first embodiment will be omitted.

[0066]FIG. 6 is a schematic sectional view of a semiconductor device according to the present embodiment. The semiconductor device 200 according to the present embodiment is a vertical MOSFET including a gate electrode inside a trench.

[0067]The semiconductor device 200 according to the present embodiment includes a silicon layer (semiconductor layer) 10. The silicon layer 10 includes an n+-type drain region 12, an n--type or n-type drift region 14, a p type body region 16, an n+-type source region 18, and a p+-type body contact region 20. The drift region 14 an n--type lower portion region (first region) 14a, an n-type intermediate region (second region) 14b, and an n--type upper portion region (third region) 14c.

[0068]In addition, the MOSFET 200 includes a first gate electrode 22, a second gate electrode 23, a first gate insulating film 24, a second gate insulating film 25, a first field plate electrode 26, a second field plate electrode 27, a first field plate insulating film 28, a second field plate insulating film 29, an interlayer insulating film 32, a source electrode 34, and a drain electrode 36. In addition, the MOSFET 200 includes a first trench 40 and a second trench 41.

[0069]In the MOSFET 200, the first gate electrode 22 and the first field plate electrode 26 are electrically and physically coupled to each other. In addition, the second gate electrode 23 and the second field plate electrode 27 are electrically and physically coupled to each other.

[0070]Thus, a gate voltage is applied to the first field plate electrode 26 and the second field plate electrode 27.

[0071]The MOSFET 200 according to the present embodiment can improve trade-off between breakdown voltage and ON resistance of a vertical transistor by the same action as in the first embodiment.

[0072]As described above, in the first and second embodiments, a case in which the first conductivity type is an n-type and a second conductivity type is a p type is used as an example, but it is also possible to use a configuration in which the first conductivity type is a p type and a second conductivity type is an n-type.

[0073]In addition, in the first and second embodiments, an example in which silicon is used as a semiconductor material is described, but it is also possible to use another semiconductor material, such as, silicon carbide (SiC), gallium nitride, or the like.

[0074]In addition, in the first and second embodiments, a case in which thicknesses of the first field plate insulating film 28 and the second field plate insulating film 29 are constant is described as an example, but it is possible to use a configuration in which the drain-source breakdown voltage is further increased by forming the thicknesses of the first field plate insulating film 28 and the second field plate insulating film 29 in a multiple stages, or by continuously changing the thickness in a depth direction.

[0075]While certain embodiments have been described, these embodiments have been presented by way of example only, and are not intended to limit the scope of the inventions. Indeed, the novel embodiments described herein may be embodied in a variety of other forms; furthermore, various omissions, substitutions and changes in the form of the embodiments described herein may be made without departing from the spirit of the inventions. The accompanying claims and their equivalents are intended to cover such forms or modifications as would fall within the scope and spirit of the inventions.

WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a semiconductor layer having a first surface and a second surface;

a drift region of a first conductivity type which is provided in the semiconductor layer;

a body region of a second conductivity type which is provided in the semiconductor layer between the drift region and the first surface;

a source region of first conductivity type which is provided in the semiconductor layer between the body region and the first surface;

a first gate electrode;

a second gate electrode which is provided interposed with the body region between the first gate electrode and the second gate elecctrode;

a first gate insulating film which is provided between the first gate electrode and the body region;

a second gate insulating film which is provided between the second gate electrode and the body region;

a first field plate electrode which is provided between the second surface and the first gate electrode;

a second field plate electrode which is provided between the second surface and the second gate electrode;

a first field plate insulating film which is provided between the first field plate electrode and the drift region;

a second field plate insulating film which is provided between the second field plate electrode and the drift region;

a first region of the first conductivity type, at least a portion of which is provided in the drift region between the first field plate electrode and the second field plate electrode;

a second region which is provided in the drift region between the first region and the body region, and has a higher impurity concentration of the first conductivity type than that of the first region; and

a third region which is provided in the drift region between the second region and the body region, and has a lower impurity concentration of the first conductivity type than that of the second region.

2. The device according to Claim 1, wherein the impurity concentration of the first conductivity type of the second region is higher than or equal to 1.5 times the impurity concentration of the first conductivity type of the first region.

3. The device according to Claim 1 or 2, wherein the second region is provided between the first field plate and the second field plate.

4. The device according to any one of Claims 1 to 3, wherein a position in which impurity concentration of the first conductivity type of the second region is the maximum is placed between two surfaces which are obtained by equally dividing a region between a surface parallel with the second surface including an end portion on the second surface side of the first field plate, and a surface parallel with the second surface including a boundary between the drift region and body region, into three regions.

5. The device according to any one of Claims 1 to 4, further comprising:

a first insulating film which is provided between the first gate electrode and the first field plate electrode; and

a second insulating film which is provided between the second gate electrode and the second field plate electrode.

6. The device according to any one of Claims 1 to 5, wherein the impurity concentration of the first conductivity type of the first region is approximately the same as the impurity concentration of the first conductivity type of the third region.

7. The device according to any one of Claims 1 to 6, further comprising:

a source electrode which is provided in the first surface and is electrically coupled to the source region; and

a drain electrode which is provided in the second surface and is electrically coupled to the drift region.

8. The device according to any one of Claims 1 to 7, wherein the semiconductor layer is a silicon layer.

ABSTRACT

According to one embodiment, a semiconductor device includes a semiconductor layer having a first surface and a second surface, a drift region of a first conductivity type in the semiconductor layer, a body region of a second conductivity type between the drift region and the first surface, a source region of first conductivity type, a first gate electrode, a second gate electrode which is provided interposed with the body region between the first gate electrode and the second gate electrode, first and second gate insulating films, a first field plate electrode between the second surface and the first gate electrode, a second field plate electrode between the second surface and the second gate electrode, a first region of the first conductivity type in the drift region, a second region which has a higher impurity concentration of the first conductivity type than that of the first region between the first region and the body region, and a third region which is provided between the second region and the body region and has a lower impurity concentration of the first conductivity type than that of the second region.

Drawings

FIG. 1

FIRST SURFACE

SECOND SURFACE

FIG. 2A

WITHOUT INTERMEDIATE REGION

WITH INTERMEDIATE REGION

DRAIN CURRENT (A/mm2)

DRAIN-SOURCE VOLTAGE (V)

FIG. 2B

WITHOUT INTERMEDIATE REGION

WITH INTERMEDIATE REGION

DRAIN CURRENT (A/mm2)

DRAIN-SOURCE VOLTAGE (V)

FIG. 3

DRAIN-SOURCE VOLTAGE (V)

ZERO

ACCELERATION ENERGY (MeV)

FIG. 4A

BOUNDARY BETWEEN DRIFT REGION AND BODY REGION

END PORTION OF FIELD PLATE ELECTRODE

n TYPE IMPURITY CONCENTRATION (atoms/cm3)

DEPTH

FIG. 4B

BOUNDARY BETWEEN DRIFT REGION AND BODY REGION

END PORTION OF FIELD PLATE ELECTRODE

WITHOUT ION INJECTION

ELECTRIC FIELD (MV/cm)

DEPTH

FIG. 5A

BOUNDARY BETWEEN DRIFT REGION AND BODY REGION

END PORTION OF FIELD PLATE ELECTRODE

n TYPE IMPURITY CONCENTRATION (atoms/cm3)

DEPTH

FIG. 4B

BOUNDARY BETWEEN DRIFT REGION AND BODY REGION

END PORTION OF FIELD PLATE ELECTRODE

WITHOUT ION INJECTION

ELECTRIC FIELD (MV/cm)

DEPTH

FIG. 6

FIRST SURFACE

SECOND SURFACE